Comparing the SEU Robustness of 6T and 8T-SER SRAM cells at 16nm

Cleiton M. Marques[1], Roberto B. Almeida[1], Cristina Meinhardt[2], Paulo F. Butzen[1].

[1]*Centro de Ciências Computacionais (C3) – Universidade Federal do Rio Grande – FURG*

[2]*Departamento de Informática e Estatística – Universidade Federal de Santa Catarina – UFSC*

{cmarques,robertoalmeida,paulobutzen}@furg.br, cristina.meinhardt@ufsc.br

***Abstract* — As technology is constantly evolving to devices on a smaller scale, project challenges begin to emerge. One of these challenges is the behavior of a circuit due to interaction with the external environment. SRAM is a key factor to performance, reliability, and power consumption of computer systems. Knowing this, analyzing the sensitivity of SRAM in relation to external effects and seek solutions to these effects is of extreme importance today. This work presents a comparison between two SRAM memory cells, evaluating the robustness to Single Event Upsets. The memory cells discussed in this work are the conventional 6T SRAM and the 8T-SER SRAM. The 8T-SER is designed to be robust to Soft Errors. A set of electrical simulations represents the collision of a charged particle individually on each sensitive node of both memory cells. Results show that the 8T-SER cell was robust in half of the test cases that it was subjected to. The 6T cell is sensitivity in all tests. However, in the case of 0->1 simulations where there was bit-flip, the 8T-SER cell presents a smaller critical charge than the 6T cell.**

Keywords — SRAM, Single Event Upset, SEU, Soft Errors, Nanometric technologies.

I. INTRODUCTION

The increased data processing required by current processors and System-On-Chip (SoCs) makes Static Random Access Memories (SRAMs) require greater storage capacities. Today it is common that SRAMs occupies 70% of the total area of high performance circuits [1]. With this, the area and energy consumption end up becoming a problem. Complementary Metal-Oxide-Semiconductor (CMOS) manufacturing technologies move increasingly to smaller scales [2]. Increasing the number of memory cells without increasing the physical space occupied. However, with this scaling, problems related to the SRAM stability begin to emerge.

In technologies below 45nm, manufacturing challenges begin to appear due to the quantum mechanics involved [3]. Working below these scales, increases the probability of permanent faults during the design process of integrated circuits [1]. It also increases the possibility of temporary faults (Soft Errors) occurring due to interference with the external environment, in cells already in functional state [4]. With the older technologies, this problem was limited only to environments hostile to radiation.

With nanometric technologies, the sensitivity of the circuits was severely affected. Thus reducing the critical charge (*Qcrit)* needed to generate an inversion of data stored in the memory cells. This effect on memory cells is denominate Single Event Upset (SEU) [5]. Thus, previously neglected low-energy particles can now cause a SEU. This makes the memories sensitive to atmospheric neutrons, as well as alpha particles, making possible the occurrence of SEU's at ground level [6]. The consequence of all this reality is the importance of studying and worrying, even at ground level, with these effects. This work intends to draw a parallel between the topology most found in the industry today, the 6T SRAM cell, in relation to the 8T-SER SRAM cell proposed to mitigate Soft Errors [7].

6T cell is widely used because it occupies a small area, has good performance and stability, and can operate at low voltage [8]. The circuit is shown in Fig. 1. The 8T-SER cell circuit is shown in Fig. 2. This cell also has good stability, acceptable performance and operates at low voltages. However, it presents a considerable increase in the occupied area. An evaluation of this cell designed in a 64nm technology is presented in [7]. Thus, the main contribution of this paper is to describe and analyze both bit-cell topologies at 16nm technological node, observing the critical charge and the cells robustness against SEU faults. In addition, compare the 64nm outcomes found in the initial evaluation [7] with the results at predictive 16nm technology node.

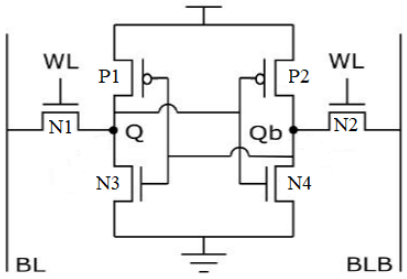

Fig. 1. 6T SRAM bit-cell.

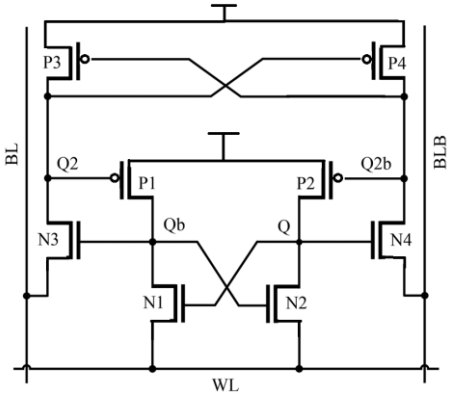

Fig. 2. 8T-SER SRAM bit-cell.

II. METODOLOGY

This section presents all details used in the analysis of the 6T and 8T-SER, respectively. The cells were evaluated taking into account the entire architecture of an 128-bit cells SRAM, using the circuits of Pre-Charge (PRE), Write Enable (WE) and Sense Amplifier Enable (SAE). The used architecture is illustrated in Fig. 3.

The evaluation was realized through the electric simulator NGSpice [9]. The circuits were described in the SPICE language, using the predictive 16nm high performance (HP) technology model [10] [11]. The main parameters of this technology are presented in Table I.

Table I – 16nm PTM High Performance bulk CMOS technology main parameter [10] [11].

Parameter		16nm
L (nm)		16
W(nm)		32
Tox (nm)		0.95
Vth0 (V)	NMOS	0.47965
	PMOS	-0.43121

The 6T memory cell was designed in the following sizing: *P1/P2/N1/N2* = 32nm and *N3/N4* = 64nm. 8T-SER in this first evaluation was designed considering all devices in the minimal sizing W= 32nm. In the future work, the transistor sizing will be explored to improve performance.

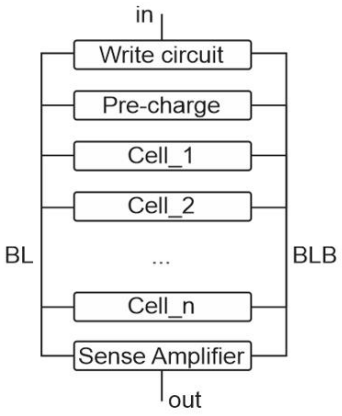

Fig. 3. SRAM column structure

To evaluate the two cells, the controls signals were defined as presented in Fig. 4. The *BIT* field can represent two different values depending on the need of the analyzer, with the respective voltage for the logic level "0" and "1", that on this 16nm technology are 0V or 0.7V, respectively. These values represent the logical value to be stored in the cell. An example with BIT=0V is shown in the Fig. 4. The Word Line control signal (*WE)* represents the state of the write circuit. When the logical value is high, it represents that the write operations is enabled. When this signal is high, the connection between the cell and the bitlines is enable. The *PRE* control signal means the state of the pre-charge circuit. This circuit is different between cells. In 6T, it is responsible for keeping the bitlines in high voltage. Already in 8T, it is responsible for grounded the bitlines. Due to this difference in functionality, when *PRE* signal is high on 6T cell, the circuit is disabled. Meanwhile, to the 8T-SER cell, when the signal is low, the circuit is disable.

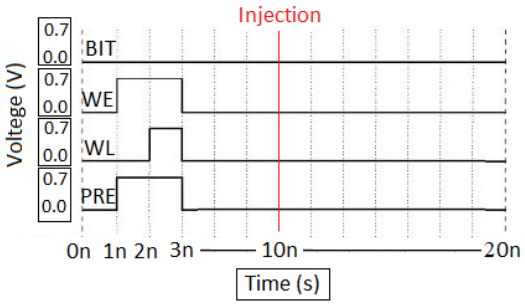

Fig. 4. Setup of the Control Signals

It is also possible to observe in the Fig. 4 the moment at which the SEU is injected. SEU is caused by the generation of charge path due to the incidence of an ionized particle in the device [12]. It is important to evaluate the sensitive nodes of both SRAMs, to identify where the behavior will be simulated. It is necessary that a particle collides with the drain terminal of a transistor and its PN-junction reversely biased, for which a voltage pulse appears on the affected node [13][14]. Thus, the sensitive nodes on the 6T bit-cell, are nodes *Q* and *Qb* from Fig.1. Whereas, for the 8T-SER bit-cell, they are nodes *Q*, *Qb*, *Q2* and *Q2b* from Fig.2.

To model the SEU effects on the circuit, a current wave was injected separately on each sensitive node. Thus, simulating the collision of a particle with that region. This wave is a double exponential and it follows the parameters described in [15], modeled with the equations (1) and (2) shown below, where *Qcrit* is the charge collected, τα is the charge time constant, τβ is the time constant to stablish the ion track and *L* is the charge collection pronfundity [16].

$$I(t) = \frac{Q_{crit}}{\tau\alpha - \tau\beta}\left(e^{-\frac{t}{\tau\alpha}} - e^{-\frac{t}{\tau\beta}}\right) \qquad (1)$$

$$Q_{crit} = 10.8 * L * LET \qquad (2)$$

The analysis consists of performing a write operation, leave the cell for a period in the hold state and then simulate an SEU on one of the sensitive nodes of SRAM. After that, it is evaluated the effects caused in the memory cell and checked whether occurs a bit-flip in the stored value. Through this analysis, it is possible to find the minimum *Qcrit* needed to cause this effect.

III. RESULTS

In this section, the data found from the simulations results is presented and discussed. Initially the results of the 6T memory cell are shown, along with its behavior when affected by SEU. Then, in the same way, the results and behavior of 8T-SER memory cell are shown. For each analysis, are presented the *Qcrit* with the Linear Energy Transfer (LET) and the current pulse (I) needed to cause a bit-flip.

For the 6T bit-cell, the results are presented in Table II. The data show that the 6T memory cell has a higher sensitivity in the 1->0 simulations. The *Qcrit* required to generate a bitflip, when the cell is storing the logical value 1, is 3.4X smaller than when the cell is storing a logical value 0. Analyzing one of the simulations, illustrated by Fig. 5

where the SEU was injected into the *Q* node, it is possible to note that the lower part of the image demonstrates the behavior of the cell sensitive nodes, when it is submitted to an electrical pulse equivalent to the possible value of *Qcrit* = 7.969 fC. This electrical pulse affects the nodes, but the nodes recover quickly. Now evaluating the upper part of the image, which also demonstrates the behavior of the sensitive nodes when submitted to the pulse, however now the pulse is increasing by one unit. The graph shows that the nodes, as expected, are affected again. However, this time, the nodes cannot recover. This result confirms that this value represents the minimum *Qcrit* capable of generating an inversion in the bit stored in the cell.

Table. II. Results of analyze of 6T SRAM.

NODO	*I(uA)*		*Qcrit (fC)*		*LET (MeV-cm²/mg)*	
	0->1	**1->0**	**0->1**	**1->0**	**0->1**	**1->0**
Q	41.924	12.129	7.970	2.305	0.369	0.107
Qb	41.924	12.129	7.970	2.305	0.369	0.107

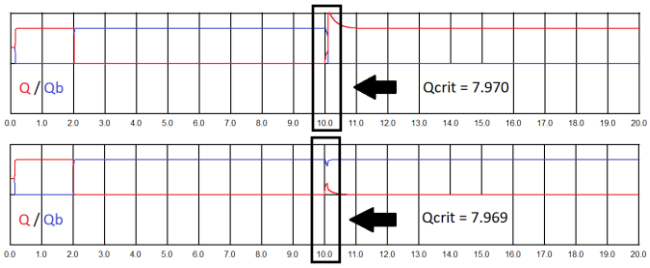

Fig. 5. SEU simulation on (Q) node in 6T SRAM.

The results of the 8T-SER bit-cell simulations are described in Table III. The data from the 8T-SER memory cell show that when sensitized, the sensitivity of the nodes are similar. Even so, there is a small difference. The Qcrit required to generate an inversion in the stored bit, when the cell is storing the logical value 0, is 11% smaller than when the cell is storing a logical value 1. The Fig. 6 shows the graphical representation of the comparison of the Qcrit required to generate the bitflip in the cells. The 8T-SER bit-cell is sensitized with a much lower Qcrit than the 6T bit-cell, to analyze it 0->1. For the 1->0 simulations, the 8T-SER presented slightly better performance, requiring a higher Qcrit for to the bitflip occur. Note that there is a large difference between sensitivity 0->1 and 1->0 in 6T cell. This is due to sizing, since the transistors *N3/N4*, responsible for ensuring the logical value 0, are a twice size of *P1/P2* (responsible for ensuring the logical value 1). However, this difference is minimal in the 8T-SER cell, since all transistors have the same size.

Table. III. Results of analyze of 8T-SER SRAM.

NODO	*I(uA)*		*Qcrit (fC)*		*LET (MeV-cm²/mg)*	
	0->1	**1->0**	**0->1**	**1->0**	**0->1**	**1->0**
Q	13.775	*Null*	2.614	*Null*	0.121	*Null*
Qb	13.775	*Null*	2.614	*Null*	0.121	*Null*
Q2	*Null*	15.505	*Null*	2.938	*Null*	0.136
Q2b	*Null*	15.503	*Null*	2.938	*Null*	0.136

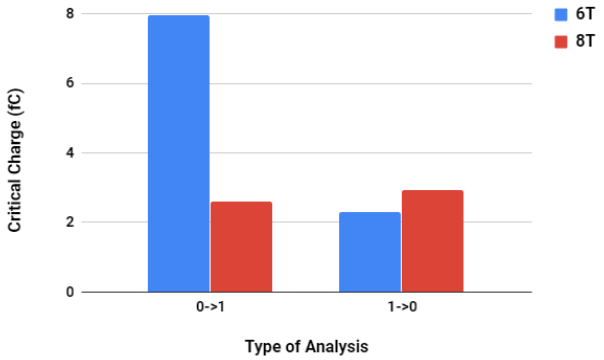

Fig. 6 *Q*crit values of 6T and 8T-SER cells.

Analyzing a simulation of the 8T cell, shown by Fig. 7, it is possible to observe that in lower part of the image, as before, it is described the behavior of the sensitive nodes. The graph shows that when the node is affected by a *Qcrit* = 2.613 fC, the cell is sensitized but can recover quickly. Looking at the top of the image, the graph also shows that, by increasing the value of *Qcrit* by one unit, the cell is affected so that it can no longer recover.

On the 8T-SER SRAM cell evaluation, a differential behavior that appeared only in the simulations of this cell is that there are cases where, independent of the intensity of the injected pulse, is not possible to find a *Qcrit*. The cell never collapsed. Fig. 8 shows this behavior and Table. III represents this effect through the Null symbology to represent this robustness behavior.

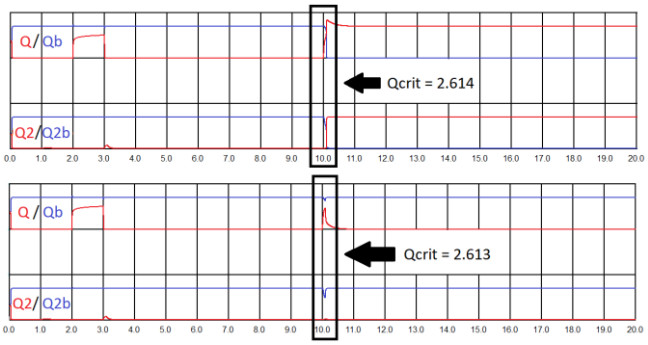

Fig. 7. SEU simulating on *Q* node in 8T-SER SRAM.

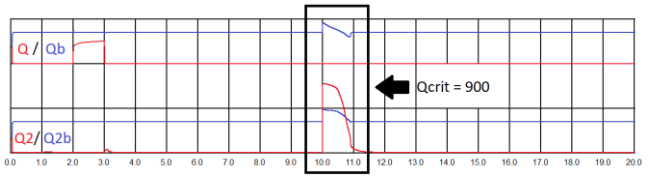

Fig. 8. SEU simulation on *Q2* node in 8T-SER SRAM.

ACKNOWLEDGEMENTS

This research is partially supported by the Brazilian National Council of Scientific and Technologic Development (CNPq), by the Brazilian Coordination of Improvement of Higher Level Personnel (CAPES) and by the Research Support Foundation of the State of Rio Grande do Sul (FAPERGS).

IV. Conclusion

This work compares the SEU robustness of the traditional 6T SRAM cell with the 8T-SER cell at 16nm technology node. The sensitive nodes of the 6T and 8T-SER cells are presented. As well the critical charge, capable of causing an inversion in the value of the stored bit, in the respective memory cells. The values demonstrate the sensitivity of SRAM's when scaled at 16nm technology. The 8T-SER cell did not reach the expected performance. Even though there are cases, where the 8T-SER cell is not compromised by the effects of the collision of a particle. This cell has twice as many sensitive nodes, what could turn out to be a problem. Does to the observed values, the 6T cell presented greater robustness in some cases. However, this occurs because the design of the 6T cell is not minimal in all its transistors.

It is important to point out that this was an initial analysis of 8T-SER cell. The sizing was considered equal and minimum for all cell transistors. Assessing more systematically its functioning and modifying certain sizes, can have significant impacts on the results found out so far. For this reason, it is important to emphasize that with future work these results will be addressed again. Also, as future works, the objective is to re-evaluate the analysis, studying the sizing of the 8T-SER cell to improve its robustness in cases where it has sensitivity.

V. References

[1] J. Samandari-Rad and R. Hughey, "Power/Energy Minimization Techniques for Variability-Aware High-Performance 16-nm 6T-SRAM," IEEE Access, vol. 4, pp. 594–613, 2016.

[2] G. Torrens, B. Alorda, C. Carmona, D. Malagon-Perianez, J. Segura, and S. A. Bota, "A 65-nm Reliable 6T CMOS SRAM Cell with Minimum Size Transistors," *IEEE Trans. Emerg. Top. Comput.*, vol. 6750, no. c, pp. 1–1, 2017.

[3] K. Bernstein et al., "High-performance CMOS variability in the 65-nm regime and beyond," IBM J. Res. Dev., vol. 50, no. 4.5, pp. 433–449, Jul. 2006.

[4] Nicolaidis, M., "Design for soft error mitigation". IEEE trans. On device and Materials Reliability 5(3), 405-418 Sep. 2005.

[5] D. Binder, E.C. Smith, and A. B. Holman, "Satellite anomalies from galactic cosmic rays," *IEEE Trans. Nucl. Sci., vol. 22, pp. 2675-2680, Dec. 1975.*

[6] Torrens, G., et al. "Analysis of current transients in SRAM memories for single event upset detection." *VLSI Circuits and Systems IV*. Vol. 7363. International Society for Optics and Photonics, 2009.

[7] SHAH, Jaspal Singh; NAIRN, David; SACHDEV, Manoj. A 32 kb macro with 8T soft error robust, SRAM cell in 65-nm CMOS. IEEE Transactions on Nuclear Science, v. 62, n. 3, p. 1367-1374, Jun. 2015.

[8] Andrei Pavlov, Manoj Sachdev, "CMOS SRAM Circuit Design and parametric test in nano-scaled technologies, Process Aware SRAM Design and Test", Springer, 2008.

[9] NGSPICE Simulator Website [Online]. Available: http://ngspice.sourceforge.net.

[10] Zhao, W.; Cao, Y. New generation of Predictive Technology Model for sub-45nm early design exploration. IEEE Trans. on Electron Devices, vol. 53, no. 11, pp. 2816-2823, Nov. 2006.

[11] Predictive Technology Model PTM [Online]. Available: http://ptm.asu.edu.

[12] B. Gill, N. Seifert, V. Zia, Comparison of alpha-particle and neutron-induced combinational and sequential logic error rates at the 32 nm technology node, in *The 2009 IEEE International Reliability Physics Symposium*, Montreal, Canada, April 26–30 (2009), pp. 199–205.

[13] Fan Wang and Vishwani D. Agrawal. Singleeventupset: Anembeddedtutorial. In VLSI Design, 2008. VLSID 2008. 21st International Conference on, pages 429–434. IEEE, 2008.

[14] RC Baumann. Soft errors in commercial integrated circuits. International Journal of High Speed Electronics and Systems,14(02):299–309,2004.

[15] S. Uznanski, G. Gasiot, P. Roche, C. Tavernier and J. L. Autran, "Single event upset and multiple cell upset modeling in commercial bulk 65 nm CMOS SRAMs and flip-flops," European Conf. on Radiation and Its Effects on Components and Systems, Bruges, 2009, pp. 194-200.

[16] MESSENGER, G. C., "Collection of Charge on Junction Nodes from Ion Tracks". IEEE Trans. of Nuclear Science, v.NS-26, n.6, Dec. 1982